**Remarks**

Claim 1 is amended. No new matter is introduced by the amendment, and entry thereof is requested.

Claims 1 - 17 and 19 - 36 are in the application, of which claims 20 - 34 were earlier withdrawn as directed to a nonelected invention. Accordingly, claims 1 - 17, 19, 35 and 36 are now under consideration.

Reconsideration of the Application, as amended, is requested.

Applicant's invention is directed to multi-package modules (MPM) including stacked first and second packages, each of which includes a die attached to a package substrate, in which the first and second package substrates are interconnected by wire bonding, and in which the first package includes a flip-chip ball grid array package having a flip-chip in a die-up configuration. Advantageously, according to the invention, the second package and the first package can be separately tested before assembly, so that second packages not testing as "good" can be discarded and only "good" second packages used in the finished MPM.

The points raised in the Office action will now be addressed.

Rejections under 35 U.S.C. § 102(b)

Claims 1 - 5, 11, 12, 17, 35 and 36 were rejected under 35 U.S.C. § 102(b) as being anticipated by Ozawa *et al.* U.S. 6,316,838 ("Ozawa"). The Examiner's reasoning is substantially the same as in an earlier Office action.

These rejections are traversed.

As Applicant pointed out in response to the earlier Office action, Ozawa does not describe or suggest a multi-package module. Ozawa describes a stacked die package having a single substrate (33), in which the substrate (33) has a flip chip die (21) attached on one face and (in Fig. 6) three stacked die ("semiconductor elements") (24), (23), (22) attached on the other face. The feature having reference numeral 24 is not a substrate; it is a semiconductor die.

Applicant's original claim 1 recited a multi-package module including stacked first and second packages, in which each said package includes a die attached to a substrate. That is, the first package has at least one die attached to a first package substrate, and the second package has at least one die attached to a second package substrate. As the application points out, this

arrangement according to the invention advantageously allows for separate testing of the packages, so that only "good" packages are used for assembly of the multi-package modules.

Addressing this argument, the Examiner asserted:

> This argument is not persuasive. First, the term "substrate" is a broad term and in light of its breadth, the element (24) in Fig. 6 of Ozawa is considered to be a "substrate" for the chip (23) in the second package. Since Ozawa provides a second substrate in the physical arrangement as claimed, it is considered to meet the structural limitations of the claims and the argument is not persuasive.

A "substrate" in the semiconductor packaging art includes at least one dielectric layer and at least one electrically conductive (metal) layer. The dielectric layer provides a surface onto which one or more die can be attached and serves to support the metal layer[s], and the electrically conductive layer is patterned and provided with pads or sites for electrical connection of the die to the substrate and pads or sites for second level interconnection of the package to a board, and/or for z-interconnection of the package to another package (as in Applicant's invention). Moreover, exposed sites or pads in the completed package can be addressed with probes for testing of the package prior to assembly in the multi-package module according to the invention. A package substrate is a "passive" device; that is, the circuitry provided by the electrically conductive layer[s] includes no active devices.

A semiconductor die would not be regarded as being a package "substrate" as that term is used generally in the semiconductor packaging art; and a semiconductor die would clearly not be within the meaning of "substrate" as that term is employed throughout Applicant's specification and drawings. Claim 1 is amended herein to recite that the substrate to which the die is attached is a passive substrate; this clearly distinguishes the die ("semiconductor element") (24) in Ozawa, as the die (24) is an active device.

Because Ozawa does not describe (or suggest) every feature of Applicant's invention as claimed, the rejection of claim 1 (and of claims depending from claim 1, and of claims 35 and 36, which incorporate claim 1) as anticipated by Ozawa should be withdrawn.

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Rejections under 35 U.S.C. § 103(a)

Claims 6 - 10, 13 and 19 were rejected under 35 U.S.C. § 103(a) for obviousness over Ozawa in view of Kakimoto *et al.* U.S. 6,333,552 ("Kakimoto"); claims 14 - 16 were rejected under 35 U.S.C. § 103(a) for obviousness over Ozawa in view of Lin U.S. 5,436,203 ("Lin").

As to claims 6 - 10, 13 and 19, Ozawa is applied as in the rejection of claim 1, and Kakimoto is relied upon (with reference to Kakimoto Figs. 3 and 7) as describing an electrical shield and an RF dic in a flip chip package. As noted above, Ozawa fails to suggest or describe a multi-package module having stacked packages and, as there is no suggestion in Kakimoto of stacked packages, Kakimoto cannot supply what Ozawa lacks. Accordingly, no combination of Kakimoto with Ozawa makes Applicant's claimed invention, and this rejection for obviousness should be withdrawn.

As to claims 14 - 16, Ozawa is applied as in the rejection of claim 1, and Lin is relied upon (with reference to Lin Fig. 1) as describing an embedded ground plane in a package substrate. As noted above, Ozawa fails to suggest or describe a multi-package module having stacked packages and, as there is no suggestion in Lin of stacked packages, Lin cannot supply what Ozawa lacks. Accordingly, no combination of Lin with Ozawa makes Applicant's claimed invention, and this rejection for obviousness should be withdrawn.

In view of the foregoing, all the claims now in the application are believed to be in condition for allowance, and action to that effect is respectfully requested

This Response accompanies a Request for Continued Examination ("RCE") which is being filed within three months following the shortened statutory period set by the Examiner for response to the Office action and, accordingly, it is accompanied by a petition for three months' extension of time and a fee or fee authorization therefor. In the event the Examiner may determine that an additional fee may be required in connection with the filing of this paper or the RCE, the Commissioner is authorized to charge any additional fee (or to credit any overpayment) to Deposit Account No. 50-0869 (CPAC 1017-5).

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PATENT

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,

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